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Analytical Calculation for Capacitances of Electrode Patterns in Touch Panels

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Abstract: In this paper, an accurate 3-dimensional (3-D) analytical solution is proposed to calculate the projective capacitances of touch panels. In this study, both simple and complex patterns were investigated for the calculation. We propose a partition strategy to divide a pattern into many rectangular or triangular sub-patterns. Each sub-pattern can be further cut into 2-D slices. The capacitance of a 2-D slice was then solved by our closed-form formulae. The total capacitance of a pattern was obtained by integrating up all the partial capacitances of the slices. In this study, the precision of our analytical method was examined by comparing the simulation results obtained from Q3D^{TM}. The results of our method had a limited deviation from the simulation results while made the computation time from one hour or some by the commercial software down to just a few tens of sec by Matlab^{TM}. In this study, the error is about 5% for simple patterns while the error was within 20% for a very complex pattern.

Keywords: touch panel, capacitor pattern, analytical solution, field-based calculation

1 Introduction

The touch panel (TP) has become the most popular user interface (UI) technology in modern smart products such as mobile phones, portable media players and personal computers. The applications of TPs are continuously extended. At present, TPs have several package structures: out-cell, on-cell and in-cell. There are five sensing techniques such as resistive [1], capacitive [2, 3], optical [4], surface wave [5] and electromagnetic methods. In industries, the projected capacitive sensing is the dominant technique for commercial products. The advantages of the projected capacitive TP are that it can support multi-touch functions and thinner, lower-cost packages with higher sensitivity and efficiency.

The projected capacitive TP utilizes electrical charges as the information carriers which are easy to interface with the electronic circuits. When the electrical charges on the sensing pads are accumulated from the driving circuit, the sensing circuit will discharge the electrical charges on the sensing pad and count how many charges by a predefined reference value. The sensitivity of the projected TP depends on the counts between touched and un-touched conditions. It is important to ensure the performance and signal reliability in the design phase for a good TP. Hence, a precise calculation for the capacitances is critically required to predict the performance of a TP accurately before manufacturing.

In industries, almost all the TP designers rely on numerical tools to calculate the capacitance of a pattern. In addition to conventional diamond structure, there were many patterns proposed to increase the sensitivity of a panel [6–17]. Lee et al. have analyzed the properties of a TP with a standard pattern of the interlocking diamond shape [18]. They utilized COMSOL Multiphysics^{TM} to assess the electric fields of two conventional electrode patterns. However, numerical techniques usually consume a lot of computing time and memory resource even for simple structures. Still, there are few physical meanings to predict possible trends or design effects from the numerical results.

For closed-form analytical calculation for most cases, conformal mapping is a suitable technique for calculations of electrostatic fields, ideal fluids, and heat flows in 2-D problems with simple boundary conditions [19, 20]. Since there are few studies by closed-form analytical solution for TPs in literature, we tried to adopt some analyt-

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ical methods which were applied for interconnects in ICs to this study [21–25].

According to the methods adopted in studies for interconnections in ICs, we proposed a quasi-3D method for the first time by integrating the analytical solutions of the 2-D slices of the projected capacitive TPs. In our calculations, the effects of electrical field shielding and charge sharing were considered and integrated.

In our previous study, our method dealt only with symmetrical structures [26]. In this study, we extended the electrode patterns to be of arbitrary shapes. By suitable partition, the closed-form formulae for symmetrical structures can be utilized for electrodes of arbitrary shapes. In this study, the calculations took two situations, touched and untouched cases, to estimate the sensitivity of a pattern.

This paper is organized as follows: In Section 2, we will explain the principles of our modeling for different TP patterns. Section 3 demonstrates the results of some selected patterns from simple to a complex shape. In this section, the results will be compared with those by numerical simulations of Q3D^{TM}. Brief discussion will be also given for each case. Section 4 gives the conclusion for this study.

2 Modeling principles

According to the development of integrated circuit (IC) technologies, there are a lot of 2-D analytical calculations for interconnects in an IC [21–27]. In our primary notion, if we can decompose the 3-D structure into many 2-D slices, we can employ these 2-D analytical methods to solve the distributions of the electric fields in a TP by integrating all the solutions of the 2-D slices. Therefore, the total capacitance of a dot on the panel can be obtained by this quasi-3-D method.

2.1 Basic interconnect structures

Let's focus first on 2-D cases. Based on the concept of finite-element method, a structure of any shape can be decomposed into many small pieces of simple shapes. Then, it can be analyzed by calculating its field equations in each partitioned area. By suitable partitioning, the properties of this structure can be approached.

With similar concepts, the electric fields between two electrodes of arbitrary shapes can be estimated by decomposing it into many small and simple structures.

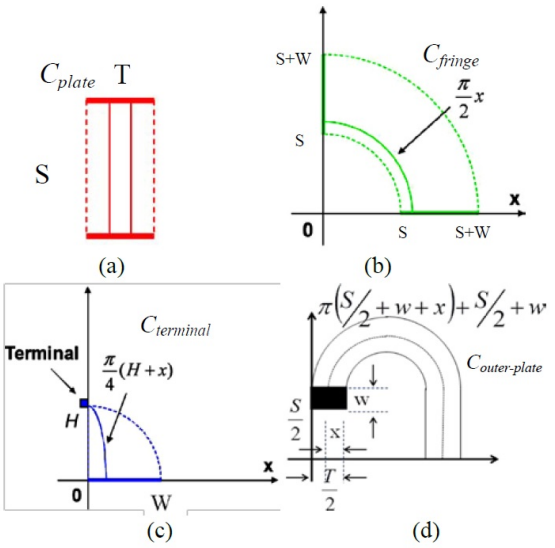

Figure 1: Four basic capacitance models: (a) plate, (b) fringe, (c) terminal, and (d) outer plate.

This thesis worked well in the studies by Zhao et al. and Zou's group for the interconnection in ICs [27–29]. In their studies, they proposed that the capacitance of any rectangular interconnect structure can be modeled and approximated by four types of basic linking models: plate, fringe, terminal, and outer plate as illustrated in Fig. 1. The symbols utilized in the derivation are also summarized in Table 1.

Table 1: Parameters for analytical calculation.

Symbol	Parameter Definitions
W	ITO width
T	ITO thickness
S	ITO spacing
H_g	Glass thickness
ϵ_0	Dielectric constant of air
ϵ_g	Dielectric constant of glass
$C_{upper-fringe}$	Fringe capacitance on the ITO
$C_{upper-terminal}$	Capacitance from ITO upper terminal
C_{plate}	Capacitance between parallel surfaces
$C_{lower-terminal}$	Capacitance from ITO lower terminal
$C_{lower-fringe}$	Fringe capacitance under the ITO
Tx	The width of transmission ITO
Rx	The width of receiving ITO
L	Triangle pattern's length

For the plate structure in Fig. 1(a), it is composed of two identical conductor edges oriented in parallel, the nor-

malized capacitance per unit length can be obtained directly with the width of the conductors and the spacing between them, i.e.

$$\frac{C_{plate}}{\varepsilon} = \frac{T}{S} \tag{1}$$

For the fringe structure, in Fig. 1(b), of two identical conductor edges oriented vertically to each other, the normalized capacitance per unit length can be obtained by conformal transformation of the plate structure or simply approximated by integrating the differential capacitance along the width of the two conductors with the corresponding spacing. As proposed by Zhao et al., the integration along simple paths would be simpler without significant loss in accuracy. The capacitance of this structure can be approximated as

$$\frac{C_{fringe}}{\varepsilon} = \int_{w=S}^{w=S+W} \frac{dw}{S} \cong \int_{x=S}^{x=S+W} \frac{dx}{\frac{\pi}{2}x} = \frac{2}{\pi}\ln(1+\frac{W}{S}) \tag{2}$$

The terminal structure in Fig. 1(c) counts on the relation between a corner and a conductor edge. The normalized capacitance can be derived as

$$\frac{C_{terminal}}{\varepsilon} = \int_{w=0}^{w=W} \frac{dw}{H} \cong \int_{x=0}^{x=H} \frac{dx}{\frac{\pi}{4}(H+x)} = \frac{4}{\pi}\ln 2 \tag{3}$$

For the links out of the back of the smaller plate to the larger plane, as shown in Fig. 1(d), the capacitance would be

$$\frac{C_{outer-plate}}{\varepsilon} = \int_{w=0}^{w=T/2} \frac{dw}{L} = \int_{x=0}^{x=T/2} \frac{dx}{\pi(S/2+W+x)+S/2+W} = \frac{1}{2\pi}\ln\left(1+\frac{\pi T}{2(1+\pi)(S/2+W)}\right) \tag{4}$$

Based on the line integrating results of the above four basic structures, the capacitances between conductors in rectangular structures can be estimated by the related formulae.

By the modeling proposed in refs. [27–29], the capacitances of several regular interconnect structures in nanometer-scaled ICs can be approximated by summing up the partial capacitance of each basic structure. According to the similarity between the metal interconnection in ICs and in TPs, it is believed that the partition method for the interconnect in ICs can also be applied on those of TPs.

2.2 Cutting electrode structures into 2-D slices

In today's TP technology, a general TP structure is composed of two parts: the indium tin oxide (ITO) traces in X and Y directions. The cross-over of the two directional traces makes an array of capacitors to sense the variations of charges around a local area on the panel. Let's take the popular diamond structure in Fig. 1 which was proposed by Apple Inc. in 2013 as the first example. As seen in Fig. 2, the red diamond electrodes are connected horizontally in X ITO traces and the blue ones are in vertical Y traces. For most commercial products, the ITO traces in both directions are grown at the same layer to form a coplanar structure. In order to prevent possible shorts between X and Y traces, bridges are introduced as shown in Fig. 3(a). Since each crossover point has four neighboring diamonds and this structure is repeated along the panel, these diamonds, as marked by a circle in Fig. 2, can be a basic unit in calculation with the repeated boundary conditions.

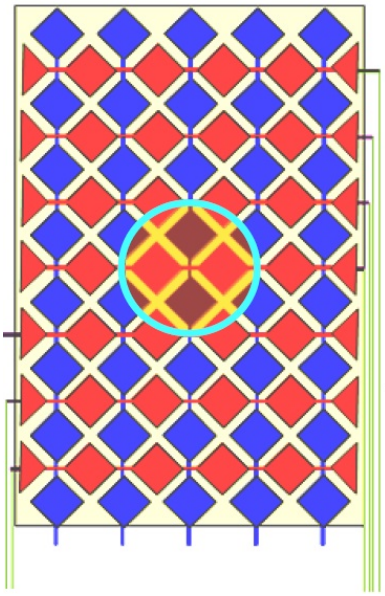

Figure 2: Top view of a diamond pattern for capacitive TPs.

Figure 3(b) depicts the cross-sectional structure along the cutting line in Fig. 3(a). We can make many slices by cutting lines on the surface in Fig. 3(a). Figure 4 illustrates our method to produce many slices of symmetrical structures. Since the electrode pattern is symmetrical in Fig. 4, we can divide this structure into the same 4 parts of the same capacitance. This step will make the calculation simpler. In the meanwhile, it should be noted that the effect of bridge was neglected in this study. For the triangular ABC

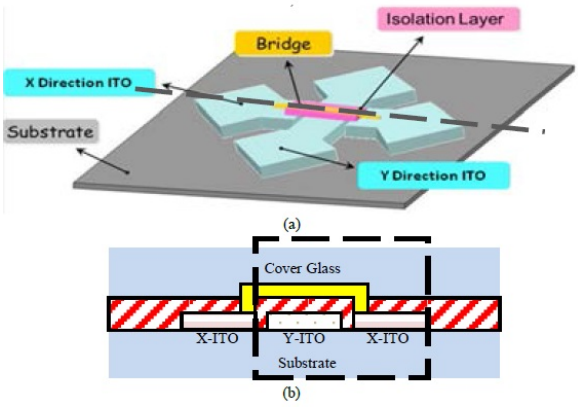

Figure 3: (a) Perspective view of the structure of the sensing pattern at the center of the marked circle in Fig. 2. A bridge is used to connect the pads of the same trace. (b) Cross-sectional view for the layer structure along the cutting line in (a). The insulate layer under the bridge is usually the same as the cover glass.

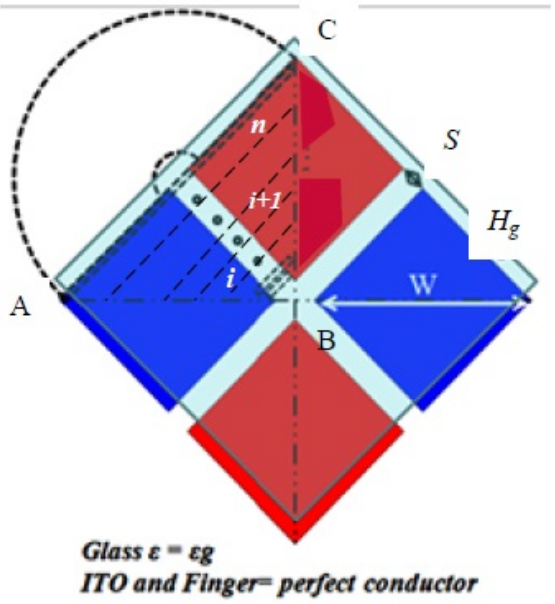

Figure 4: Cutting for symmetrical slices in triangle ABC for the diamond pattern.

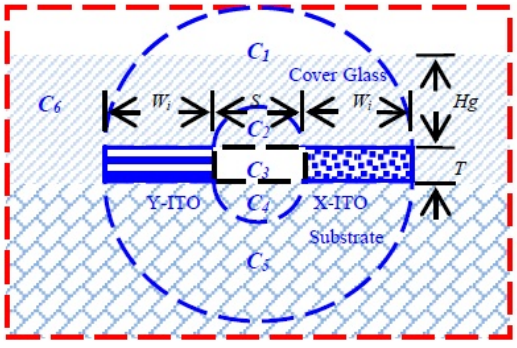

Figure 5: Extended cross-sectional view of the basic slice marked by the dashed rectangle in Fig. 3. This structure can be divided into 6 parts. The geometry parameters are also denoted.

in Fig. 4, we can cut further to make the X- and Y-ITO in each slice have the same geometry. However, it should be noted that the width of the conductors in every slice, W_i, will change from one slice to another.

For each cutting line, the related cross-sectional structure will look like that in Fig. 5. After the capacitance of a 2-D slice in Fig. 5 is obtained, the total capacitance in Fig. 4 can be obtained by integrating all partial slice capacitances. The 2-D slice as shown in Fig. 5 was the structure basis in our calculations. We tried to partition all electrode patterns in this study and cut them into the basic slice as in Fig. 5 with different geometry parameters.

2.3 Calculation for 2-D symmetrical structures

For the basic 2-D slice as shown in Fig. 5 and Fig. 6(a), there are 6 parts to be calculated. Since it is still a symmetric structure, it can be folded by regarding there is a vertical conducting plan in the center. We can calculate the partial capacitances for a half part as shown in Fig. 6(b). Therefore, C_1 in Fig. 5 is 1/2 of $C_{upper-fringe}$ in Fig. 6(b). In this figure, one can recognize C_1 is equal to a serial connection of two fringe structures as in Fig. 1(b). Therefore, we can denote the related capacitance as $C_{upper-fringe}$ as show in Fig. 6(b). The other partial capacitances in Fig. 6(b) can be analyzed in the same way. All the capacitance values from C_1 to C_6 can be derived from the corresponding results in Fig. 6(b) by half.

It should be noted that there might be different dielectrics in an area which will make the calculation a little complex. For example, the area for C_1 in Fig. 5 may contain cover glass and air if the thickness of the cover glass, *Hg*, is less than the width of the electrode, *W*. Therefore, eqs. (1)-(4) are too simple to be applied for TP structures. The problems will be solved in the next sections.

2.4 Partial capacitances for the basic slice

For the structure in Fig. 5 or Fig. 6(b), let's assume all the coplanar conductors are surrounded by the same dielectric material, for example $\varepsilon_{dielectric}$. According to the partition in Fig. 6(b), the total capacitance C for the basic struc-

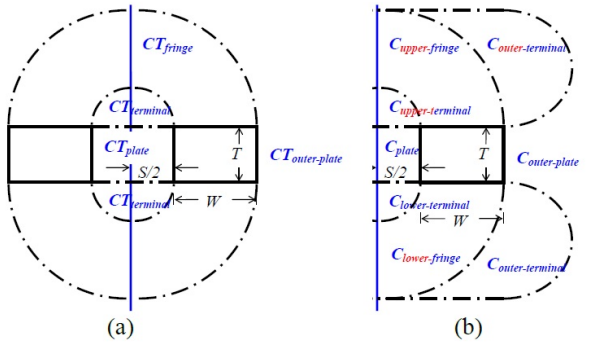

Figure 6: (a) Dimensions and partial capacitances for the basic slice in Fig. 5 with two identical conductors in parallel. (b) Partitions for the half structure by Zhao's models. The adopted models are also indicated in the subscripts.

ture in Fig. 5 can be derived by

$$\frac{C}{\varepsilon_{dielectric}} = \frac{1}{2}\frac{1}{\varepsilon_{dielectric}} \left(\begin{array}{l} C_{upper-fringe} + C_{upper-terminal} + C_{plate} + C_{lower-terminal} \\ +C_{lower-fringe} + C_{outer-plate} + 2C_{outer-terminal} \end{array} \right) \tag{5}$$

It should be noticed that $C_{upper-terminal}$ cannot be obtained simply by eq. (3) due to its different linked area. To account for the charge distribution and to compensate the field distortion due to adjacent plate and fringe capacitances, Zhao et al. [27, 28] proposed an empirical approximation for these two corners, i.e.

$$\frac{C_{lower-ter\,min\,al}}{\varepsilon} \cong \frac{2}{\pi} \tag{6}$$

and

$$\frac{C_{upper-ter\,min\,al}}{\varepsilon} \cong \frac{1}{\pi} \tag{7}$$

Therefore, the total capacitance for the basic slice in Fig. 5 or Fig. 6(a) is

$$\frac{C}{\varepsilon_{dielectric}} = \frac{T}{S} + \frac{2}{\pi}\ln\left(1+\frac{2W}{S}\right) + \frac{3}{\pi} + \frac{1}{\pi}\ln\left(1+\frac{\pi T}{2(1+\pi)(S/2+W)}\right) \tag{8}$$

For the TP structures, however, the dielectric layers are different above and below the ITO conductors. The above formulae should be modified. In our calculation, the dielectric constant was taken as a variable along the integrating path in eqs.(1)-(4). The derived partial capacitances for the basic slice in Fig. 6(b) are summarized in Table 2 [26, 30]. For present study, the interface effect on the flow lines of electric fields was neglected. In Table 2, $\varepsilon_{eff-fringe}$ and $\varepsilon_{eff-termianl}$ are effective dielectric constants by considering the field flow lines passing through glass and the air.

2.5 Calculation for symmetrical structures

We calculated for two situations: untouched and touched. In general, the dimensions of a capacitive sensing pattern need to take that of a human's finger into consideration. For a too large capacitive sensor on the panel, the user's finger will touch over less than a dot unit. In this case, the sensitivity and linearity of the TP would be deteriorated. On the other hand, it is not cost effective to make the dots on the panel too small. For most commercial products, the dimensions of a capacitive sensor dot are designed to be at least 50% of the width of a finger. Therefore, in this study, we assumed the basic slice was in a size that can be covered by one finger only. In our calculations, a finger on the panel was represented by a grounded post to be placed on the cover glass.

The basic structure in our calculation can be represented in Fig. 7. Fig. 7(a) depicts the schematic structure for the untouched situation. Fig. 7(b) emulates the touched situation. The finger was modeled as a grounded metallic post on the surface. Due to the redistribution of electric fields under the finger, the integration range will be confined under the finger. Therefore, the partitions for the basic structure under untouched and touched situations will be different.

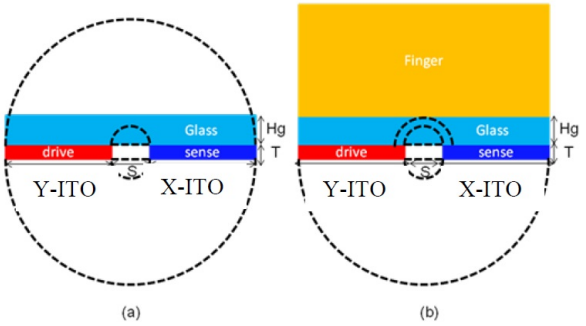

Figure 7: Schematic structures for (a) untouched and (b) touched situations.

Figure 8 illustrates more detailed partition and shows the scenario of the touched case. In this case, some coupling effects become prominent. When the finger touches on the cover glass, the distribution of the electrical fields will change. Figure 9 depicts the effects of field shielding and charge sharing as the following.

The first is field shielding as illustrated in Fig. 9(a) which the effective coupling area between the two ITO surfaces is reduced by the approaching of an additional finger. The second is charge sharing as in Fig. 9(b). When there are multiple conductors, the flow lines of the electric fields

Table 2: Closed-form formulae for partial capacitances in Fig. 6(b).

Partial Capacitance	For uniform ϵ	For untouched TPs with air ϵ_0 and glass ϵ_g	For touched TPs with air ϵ_0 and glass ϵ_g and a pod
$C_{upper-fringe}$	$\frac{\epsilon}{\pi}\ln\left(1+\frac{W}{S/2}\right)$	$\begin{cases}\epsilon_0\epsilon_g\frac{1}{\pi}\ln(1+2W/S), & \text{for } H_g < S/2+W\\ \epsilon_0\epsilon_g\frac{1}{\pi}\ln\left(1+\frac{H_g-S/2}{S/2}\right)\\ +\frac{1}{\pi}\epsilon_{eff-fringe}\epsilon_0\ln(1+\frac{W+H_g+S/2}{S/2}) & \\ \text{for } H_g \geq S/2+W\end{cases}$	$\epsilon_0\epsilon_g\left(\frac{1}{\pi}\ln\left(\frac{(S+2W_1)(S+2H_g/pi)}{S(S+2H_g/pi+2W_1)}\right)\right)$
$C_{upper-terminal}$	$\cong\frac{\epsilon}{\pi}$	$\begin{cases}\epsilon_0\epsilon_g\frac{1}{\pi}, & \text{for } H_g \geq S/2\\ \epsilon_{eff-terminal}\epsilon_0\frac{1}{\pi}, & \text{for } H_g < S/2\end{cases}$	$\epsilon_0\epsilon_g\left(\frac{(\frac{2}{\pi}\ln(1+1.297H_{g1}/S))^2}{\frac{2}{\pi}\ln(1+1.2974H_{g1}/S)+\frac{4}{\pi}\ln(1+0.3244S/H_g)}\right)$
C_{plate}	$\epsilon\frac{T}{S}$	$\epsilon_0\frac{T}{S}$	$\epsilon_0\left(\frac{T}{S}-\frac{2}{\pi}\ln\left(\frac{H_g+2S/\pi+T_1}{H_g+2S/pi}\right)\right)$
$C_{lower-terminal}$	$\cong\frac{2\epsilon}{\pi}$	$\frac{\epsilon_0}{\pi}$	$\frac{\epsilon_0}{\pi}$
$C_{lower-fringe}$	$\frac{\epsilon}{\pi}\ln(1+\frac{W}{S/2})$	$\frac{\epsilon}{\pi}\ln(1+\frac{W}{S/2})$	$\frac{\epsilon}{\pi}\ln(1+\frac{W}{S/2})$
$C_{outer-plate}$	$\approx 2\cdot$ eq. 4	$\left(\frac{\epsilon_0+\epsilon_{eff-terminal}}{2}\right)\frac{1}{\pi}\ln\left(1+\frac{\pi T}{2(1+\pi)(S/2+W)}\right)$	$\frac{\epsilon_0}{2}\frac{1}{\pi}\ln\left(1+\frac{\pi T}{2(1+\pi)(S/2+W)}\right)$
$C_{outer-terminal}$	$\cong\frac{\epsilon}{\pi}$	$\cong\frac{\epsilon}{\pi}$	$\cong\frac{\epsilon}{\pi}$

Note:

1. $\epsilon_{eff-fringe}=1+\frac{\epsilon_g H_g}{S/2+W}$ 2. $\epsilon_{eff-terminal}=1+\frac{\epsilon_g H_g}{S/2}$ 3. $H_{g1}=\min(H_g, S/2)$ 4. $T_1=\min(T,\sqrt{S^2+H_g^2}-H_g)$

$$W_1=\begin{cases}\min(W, H_g-S/2), & \text{for } H_g \geq S/2\\ 0 \text{ for } H_g < S/2\end{cases}$$

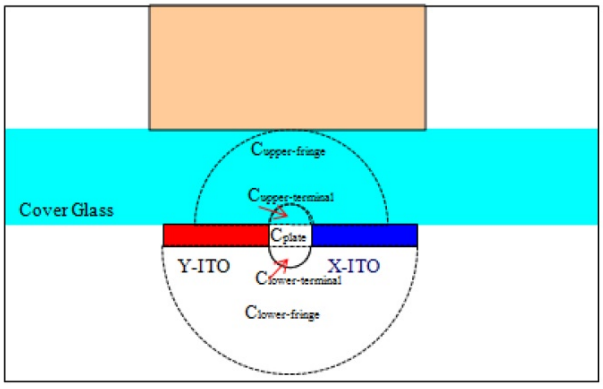

Figure 8: Partition for partial capacitances for the touched situation.

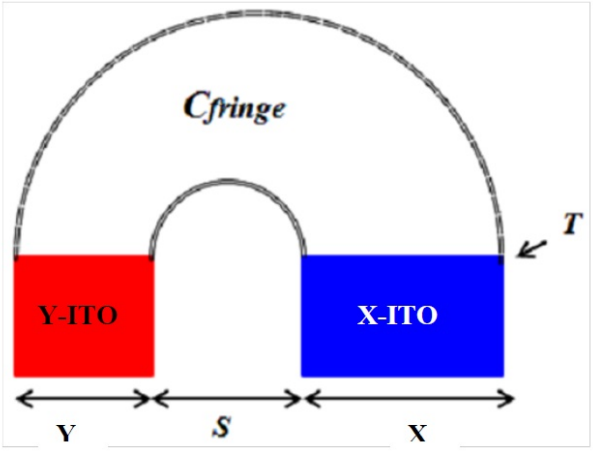

Figure 10: Another basic structure with asymmetrical trace widths of X and Y.

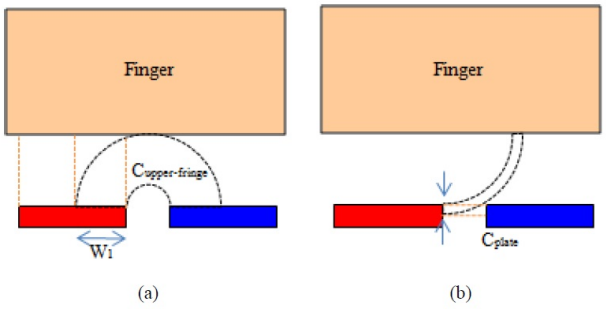

Figure 9: The integration paths change due to the effect of (a) field shielding and (b) charge sharing.

may diverge to neighboring conductor surfaces rather than a single surface.

In Fig. 8, there are five parts to be calculated. For convenient calculation, the finger was presumed as an infinite ground plane to simplify the mathematical forms of the partial capacitances. Therefore, the integration for every partial capacitance needed to be recalculated to count the effect of the finger. The derived formulae are summarized in Table 2.

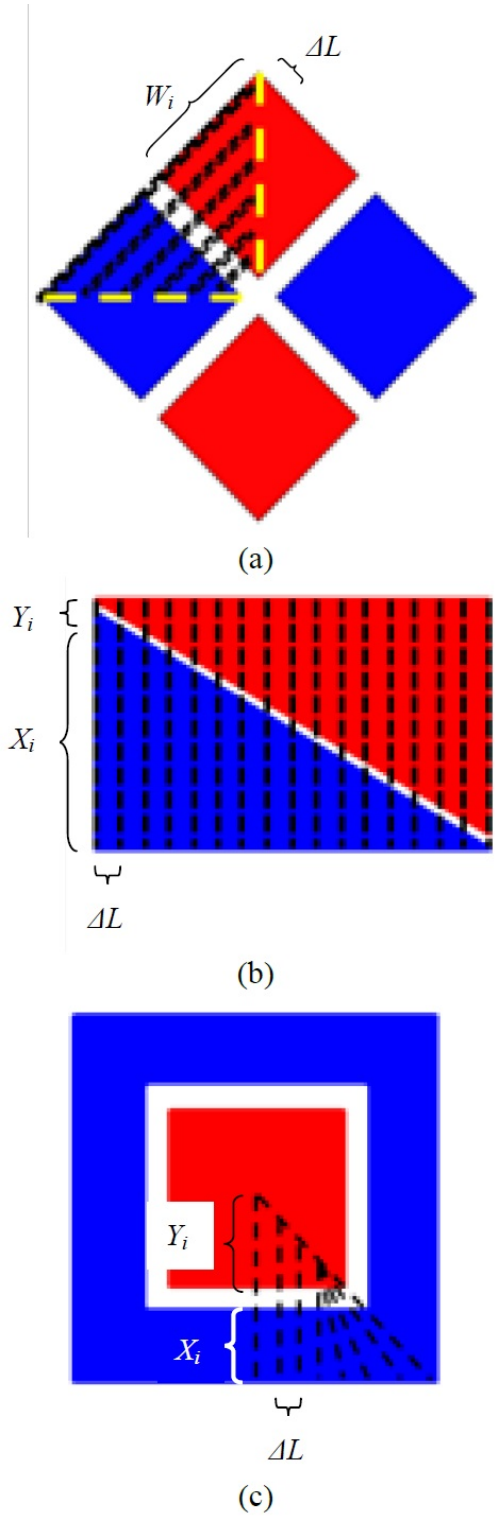

Figure 11: Slicing strategies for (a) diamond pattern, (b) triangle pattern, and (c) concentric square pattern.

2.6 Calculation for asymmetrical structures

The above discussion deals only for the basic structure of two ITO traces of the same widths. By suitable transformation, our formulae in Table 2 can also be applied for asymmetrical structures. For the asymmetrical structure as shown in Fig. 10 with unequal widths, we can employ suitable transformation of the unequal-width structure to utilize the formulae in Table 2 by an effective width [27]. And the effective width, W, in Table 2 should be expressed as

$$W = \frac{\left(\sqrt{XY(X+S)(Y+S)} + XY\right)}{(X+Y+S)}, \tag{9}$$

where X and Y represent the widths of the two ITO pads in a slice.

Therefore, with the transformation by eq. (9), we can also utilize the same formulae in Table 2 by making slices of asymmetrical structures for electrode patterns. The basic structure and the formulae in Table 2 were used for calculation of the patterns in our study.

2.7 Slicing/Integration strategies

In this study, five patterns from simple to complex were chosen for the investigation. Figure 11 depicts the slicing strategies for 3 simple patterns to make sliced pieces have a basic structure as shown in Fig. 5 or Fig. 10. For each slice with its capacitance per unit length, the total capacitance for an electrode pattern in Fig. 11 can be integrated as the following.

For the diamond pattern in Fig. 11(a), the slice capacitance can be denoted as $C(W_i)$, its total capacitance can be calculated as

$$C_{total} = \int C(W_i)dL \cong \sum_{i=1}^{N} C(W_i)\Delta L \tag{10}$$

For the triangle pattern as show in Fig. 11(b), the total capacitance can be approximated as

$$C_{total} = \int C(X_i, Y_i)dL \cong \sum_{i=1}^{N} C(X_i, Y_i)\Delta L \tag{11}$$

With the transformation by eq. (9), one can use the formulae in Table 2 easily to obtain the total capacitance.

The slicing strategy was a little complex for the concentric square pattern proposed by Yu et al. [9] in Fig. 11(c). Figure 12(a) shows our strategy by dividing the pattern into two parts. For part I, we cut this part into asymmetric slices, as depicted in Fig. 12(b).

For part II, the sliced pieces are triangles denoted as the original slice in Fig. 12(c). To calculate its capacitance, the direct way is to recalculate the line integrations for the related partial capacitances in a way similar to those in eqs.(1)-(4) [31]. We can transform the original slice to a triangular slice as the reformed slice in Fig. 12(c) by presuming the capacitances of both slice are very close. In addition, if the lengths X_i and Y_i in Fig. 12(c) are similar, the capacitance of the reformed slice can be approximated by half of the capacitance of the basic slice as the slice III in Fig. 12(c). Therefore, by suitable partition without losing too much accuracy, the original triangular slice in Fig. 12(c) can be reformed by regarding it as a symmetrical triangular slice. Therefore, the capacitance of slice II C_{i_tr} is presumed to be close to C_i. And C_{i_tr} is roughly half of the capacitance of the basic structure, slice III.

In our study, the number of triangular slices was not many. The accumulated error in the calculation for triangular parts can be controlled in a limit.

With the basic slice, symmetric or asymmetric, and the triangular slice, we can divide an electrode pattern into a combination of rectangular and triangular patterns. The partition strategy for complex patterns will be shown directly in the next section.

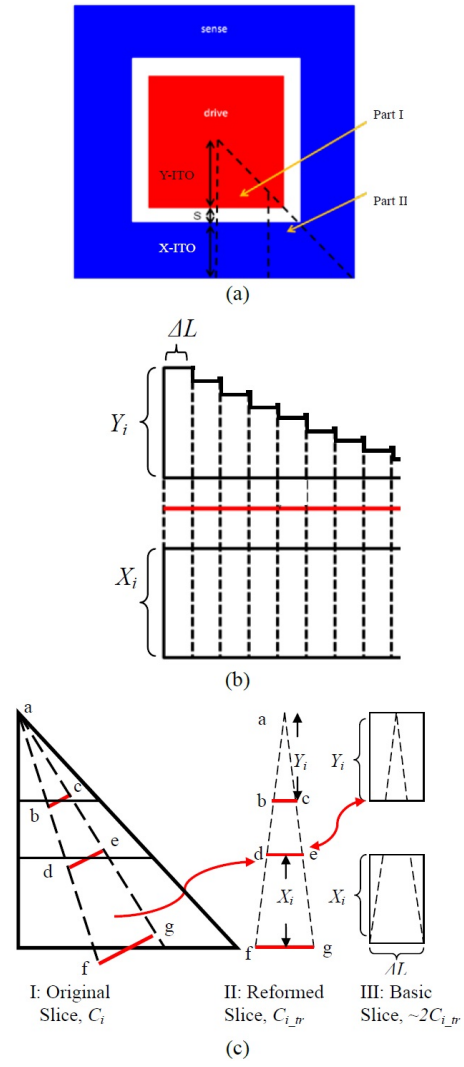

Figure 12: Slicing strategies for concentric square pattern. (a) The pattern is divided into two parts. (b) Slicing for part I. (c) Slicing for part II. The original slice (I) can be approximated by reforming it to a symmetrical triangular shape (II). This reformed slice can be estimated by calculating the capacitance of slice III. If $X \sim Y_i$, the formulae in Table 2 can be applied.

3 Results and Discussion

In this study, five TP electrode patterns were selected to investigate the precision of our analytical calculation. In addition to the mentioned diamond, triangle, and concentric square patterns in previous section, two special patterns proposed by HTC Inc. [10] and Raydium Semiconductor Inc. [12, 14] were also investigated.

Our calculation was performed by Matlab™. The precision of our method was verified by comparing the simulation results by Q3D™ which is popular in industries for estimating the capacitance of TPs.

In this study, the capacitance of the bridge in each pattern was not considered due to its little effect on the sensitivity, ΔC. The sensitivity is defined as the difference between the capacitance without touch, C_{UT}, and that under touch, C_T.

3.1 Diamond pattern

As indicated in Fig. 11(a), the slicing strategy makes each slice having the symmetrical structure as in Fig. 6. Figure 13 also shows five structural variables that can be adjusted, i.e. W, S, T, H_g and ϵ_g.

In this calculation, S was less than 100 nm for optical requirements. T was less than 1 μm for ITO layers. For all the cases in this study, H_g was selected as 0.7 mm. And ϵ_g was selected as 7 for tempered cover glass.

Fig. 14 demonstrates the comparison of the analytical calculation with the numerical simulation by Q3D™. As seen in this figure, both the analytical and numerical results are very close. In this calculation, the maximal deviation between two results was within 3%. Comparison

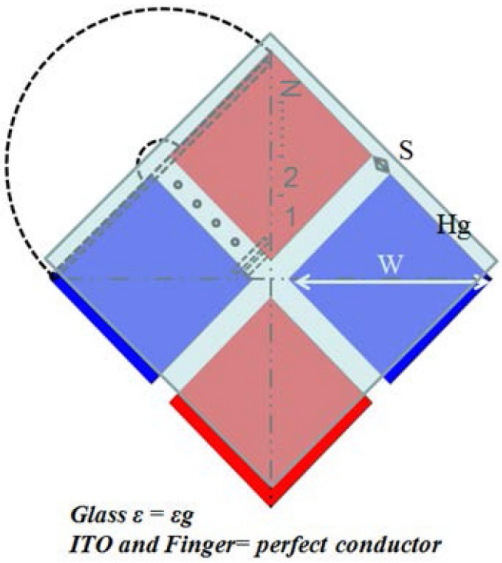

Figure 13: Structural parameters for the diamond pattern.

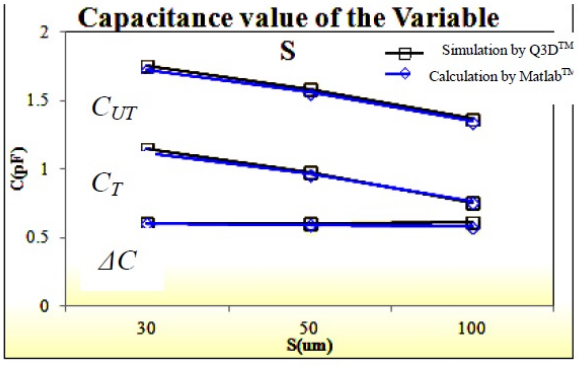

Figure 14: Comparison of C_{UT}, C_T, and ΔC for the diamond pattern as a function of spacing, S. The analytical calculation results are also compared with those simulation results by Q3D™. In this case, W = 5 mm, T = 1 µm.

for other parameters was also studied in our previous report [26].

3.2 Triangular pattern

Figure 11(b) indicates the strategy of slicing for the triangular pattern. Figure 15 shows the structural parameters that can be changed in this investigation.

The selected parameters are similar to those for the diamond pattern and indicated in Fig. 16. While estimating the effects of other parameters on the capacitances, W = 5 mm, and L = 20 mm. As seen in Fig. 16, the deviation between our analytical calculation and the numerical results is within 5%. In this case, L was fixed as 20 mm while W was changed from 2.5 mm down to 1 mm. It can

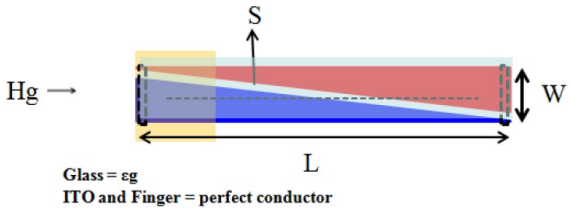

Figure 15: Structural parameters for the triangular pattern.

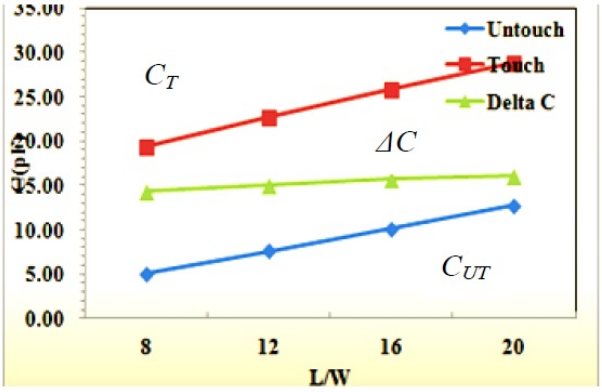

Figure 16: Effect of dimension ratio L/W on C_{UT}, C_T, and ΔC for the triangular pattern. In this case, L = 20 mm, S = 30 µm, and T = 1 µm.

be confirmed that the transformation by eq. (9) is good for the calculation for the triangular patterns.

3.3 Concentric square pattern[9]

The structural parameters for the concentric square pattern were indicated in Fig. 17 for this calculation. Figure 18 is the effect of dimensional ratio of Tx/Rx where we kept the total length W = 5 mm. In this figure, it should be noted that the maximal deviation between the analytical results and the simulation results is 5%.

As seen in Fig. 18, the worst case may be found for small Tx/Rx ratio. The precision of the analytical calculation is good for Tx/Rx larger than 4. In this figure, the capacitances of C_U and C_{UT} are underestimated as compared to those by numerical calculation. Even our calculation may arise more errors, it seems that the sensitivity ΔC can tolerate smaller Tx/Rx ratio down to 1 or 2. This finding indicates our approximation in Fig. 12 would result in larger errors in the calculation. One should be careful while making a triangular sub-pattern as in Fig. 12. For partitions keeping Tx/Rx higher than 2, the precision of the analytical calculation can still be acceptable.

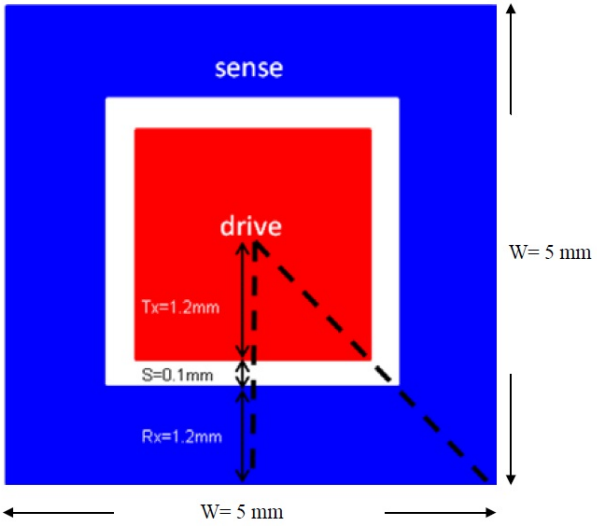

Figure 17: Structural parameters for the concentric square pattern.

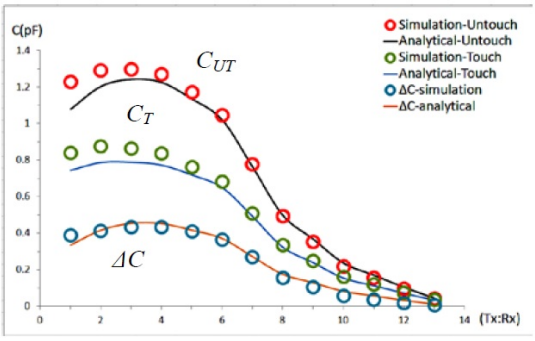

Figure 18: Effect of dimension ratio Tx/Rx on C_{UT}, C_T, and ΔC for the concentric square pattern. In this case, $W = 5$ mm, $S = 100$ μm, $T = 0.1$ μm.

3.4 Hexagonal pattern[10]

This pattern was proposed by HTC Inc. in 2013. In Fig. 19, the structural parameters and the partition strategy are indicated. As indicated in this figure, by suitable partition, this pattern can be divided into many rectangular and triangular sub-patterns. By this partition strategy, the formulae in Table 2 can be employed for these sub-patterns to calculate the total capacitance. Figure 20 shows the effect of dimensional ratio of Tx/Rx. In this figure, it should be noted that the maximal deviation between the analytical results and the simulation results is 5%.

As seen in Fig. 20, similar results can be found as in Fig. 18. Capacitances C_U and C_{UT} by our calculation are a little lower than those by numerical calculation. However, the sensitivity ΔC can tolerate a wider range of geometry ratios. While checking the partition in Fig. 19, we may attribute that most of the errors come from the triangular sub-patterns. In this case, the approximation in Fig. 12 still works fine with a 5% deviation from the numerical calculation.

3.5 Complex pattern[Y07,Y09]

In addition to HTC's pattern, we also investigate a rather complex pattern proposed by Raydium Semiconductor Inc. In Fig. 21, the structural parameters and the partition strategy are indicated. Since this pattern is complex, the partition lines in this figure divide this pattern into many fragments or sub-patterns. Figure 22 compares the results from the analytical calculation and the numerical simulation as a function of the length of the hand. In this figure, the largest deviation between the results by the two tools was around within 20%.

The larger error may be attributed from the calculation of triangular sub-patterns. As checking our partition in Fig. 21, one can find there are many triangular sub-patterns with a smaller geometrical ratio for Tx/Rx in Fig. 18. These triangular sub-patterns may deteriorate the resulted precision of the calculation.

This finding may indicate that our partition strategy is not very efficient for this complex pattern even our analytical results are still close to those by numerical simulation. If we can reduce the number of triangular sub-patterns, it is believed the precision of our analytical calculation can be improved. Nevertheless, our findings from the results of different patterns would convince us that our analytical calculation has a precision competing to commercial numerical tools.

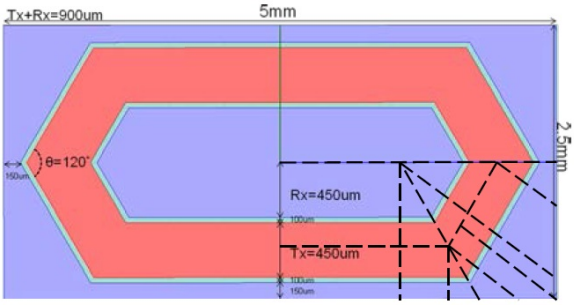

Figure 19: Structural parameters for the hexagonal pattern. The dashed line indicates how this pattern was divided and calculated with different slice structures.

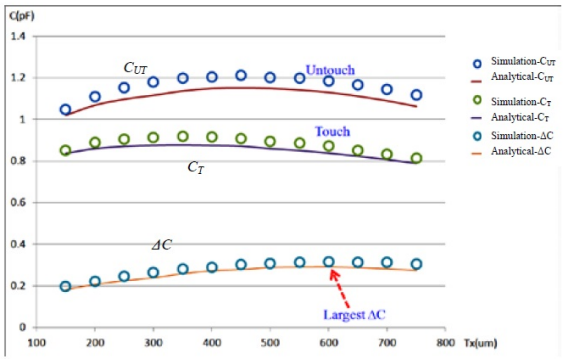

Figure 20: Effect of dimension ratio Tx/Rx on C_{UT}, C_T, and ΔC for the hexagonal pattern. In this case, Tx+Rx= 0.9 mm. The other parameters can be found in Fig. 19.

3.6 Discussion

According to the above results in Figs. 12–22, it can be found that our calculations were accurate enough and can compete to commercial software tools which utilizing numerical techniques.

With our analytical formulation and partition strategies, it is convenient for designers to evaluate the quantitative properties and the effects of design parameters of a TP pattern. Especially, the computing time was largely reduced from several hours to some tens of seconds for the same structure. Since the analytical method costs little computational resource, this method is suitable for quick evaluation of effects of design parameters in the early stages of designing an ITO pattern. In other words, an optimal set of factors can be obtained by our analytical method.

4 Conclusion

This paper presents a field-based model with partition strategies to calculate the capacitances of TPs from simple patterns to a complex structure. The formulae for basic slices were derived. For complex patterns, one should be careful to make triangular sub-patterns to control the precision of the analytical calculation. By comparing with the results of Q3D^{TM} simulations for the same TP pattern, our analytical model demonstrated an excellent accuracy for the capacitance calculation.

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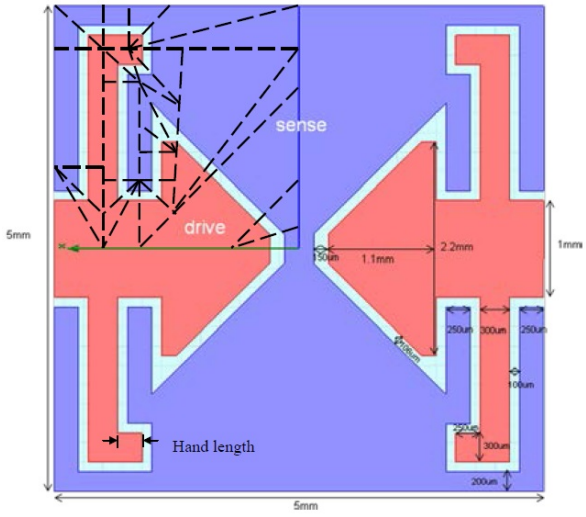

Figure 21: Structural parameters for the selected complex pattern. The dashed line indicates our partition strategy to divide this pattern into many triangular and rectangular sub-patterns.

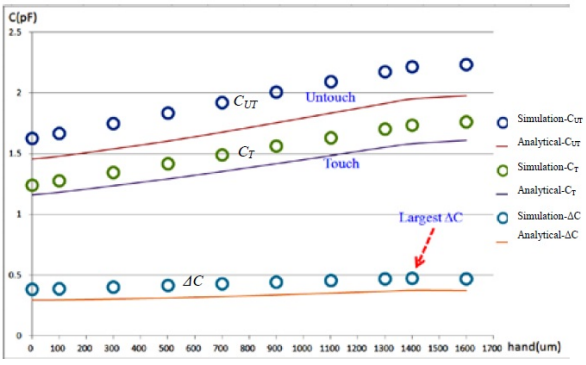

Figure 22: Effect of the length of the hand in Fig. 20 on C_{UT}, C_T, and ΔC for Raydium complex pattern. In this case, the employed parameters are noted in Fig. 21.

References

[1] R.N. Aguilar and G.C.M. Meijer, "Fast interface electronics for a resistive touch screen," in Proc. IEEE Sensors, vol. 2, pp.1360-1363, 2002.

[2] S. P. Hotelling, J. A. Strickon, and B. Q. Huppi, "Multipoint touch screen," U.S Patent 7, 663, 607, Feb. 16, 2010.

[3] S. P. Hotelling and B. R. Land, "Double-sided touch-sensitive panel with shield and drive combined layer," U.S. Patent 7, 920, 129, Apr. 5, 2011.

[4] S. H. Bae, B. C. Yu, S. Lee, H. U. Jang, J. Choi, M. Sohn, I. Ahn, and I. Kang, "Integrating Multi-Touch Function with a Large-Sized

LCD," SID Int'l Symposium Dig. Tech. Papers, pp. 178-181, 2008.
[5] T. J. Knowles, "Touch panel for an acoustic touch position sensor," U.S Patent 5, 329, 070, Jul. 12, 1994.
[6] C. Y. Chang, S. T.Chien, F.Z.Zhang, "Conductor pattern structure of capacitive touch panel," E.P. Patent 2 650 764, Oct. 16, 2013.
[7] Y. K. Hong, H. B. LEE, K. S. CHAE, S. H. Ji, D. S. Yoo, B. C. Lee, S. J. Nam, "Touch panel," U.S. Patent 0 267 228, Oct. 25, 2012.
[8] H. S. Yu, "Sensor for Capacitive Touch Panel Including Mesh Pattern and Capacitive Touch Panel Including the Same," U.S. Patent 0 299 865, Nov. 29, 2012.
[9] R. W. Wang, H. L. Ye, J. Yu, "Touch-control pattern structure, manufacture method thereof and touch panel containing therein," E.P. Patent 2 527 960, Nov. 28, 2012.
[10] P. L. Lo, Y. C. Lin, Y. F. Hsueh, T. M. Chen, "Touch panel," E.P. Patent 2 639 681 , Sep. 18, 2013.
[11] W. H. Ho, Y.C. Chen, Y. C. Lin, "Single-layer and multi-touch projected capacitive apparatus," U.S. Patent 0 206 379, Aug. 16, 2012.
[12] S. F. Wang, K. P. Lee, "Electrode unit with perimeter-lengthened touch-sensing pattern for touch-sensing element located at fringes of touch panel," U.S. Patent 0 241 851, Sep. 19, 2013.
[13] S. J. Kang, K. U. Kim, W. J. Baek, "Electrode pattern for touch screen, driver for touch screen, and touch screen," U.S. Patent 0 080 353, Apr. 7, 2011.
[14] S. F. Wang, "Electrode unit with perimeter-lengthened touch-sensing pattern for touch-sensing element located at fringes of touch panel," U.S. Patent 0 240 342, Sep. 19, 2013.
[15] J. Y. Chou, C. Y. Yeh, J. L. Chou, C. K. Lin, C. J. Teng, C. H. Su, "Touch-sensing panel and touch-sensing display apparatus," U.S. Patent 0 194 213, Aug. 1, 2013.
[16] Y. S. Kim, Y. J. Kim, H. Y. Song, H. J. PARK, "Sensing electrode pattern of touch panel," U.S. Patent 0 162 545, Jun. 27, 2013.
[17] K. S. Lee, J. Y. Lee, "Touch screen panel," U.S. Patent 8 558 805, Oct. 15, 2013.
[18] Jeffrey Lee, Matthew T. Cole, Jackson Chi Sun Lai, and Arokia Nathan, "An Analysis of Electrode Patterns in Capacitive Touch Screen Panels," J. Display Technol., vol. 10(5), pp.362-366, 2014.
[19] Alan Jeffrey "Advanced Engineering Mathematics," Academic Press, 2001.
[20] S. M. Sharma, S. Dasgupta, and M. V. Kartikeyan, "Successive Conformal Mapping Technique to Extract Inner Fringe Capacitance of Underlap DG-FinFET and Its Variations With Geometrical Parameters," IEEE Tran. Electron. Dev., vol. 64, no. 2, pp. 384-391, 2017.
[21] J. H. Chern, J. Huang, L. Arledge, P.-C. Li, and P. Yang, "Multilevel metal capacitance models for CAD design synthesis systems," IEEE Electron Device Lett., vol. 13, no. 1, pp. 32-34, Jan. 1992.
[22] T. Sakurai, "Closed-form expressions for interconnection delay, coupling, and crosstalk in VLSI's," IEEE Trans. Electron Devices, vol. 40, no. 1, pp. 118-124, Jan. 1993.
[23] U. Choudhury and A. Sangiovanni-Vicentelli, "Automatic generation of analytical models for interconnect capacitances," IEEE Trans. Comput.-Aided Design Integr. Circuits Syst., vol. 14, no. 4, pp. 470-480, Apr. 1995.
[24] S.-P. Sim, N. D. Arora, C. Cao, S. Krishan, K. Lee, and C. Y. Yang, "Analytical capacitance model for high-speed interconnects with diagonal routing," Proc. IEEE Interconnect Tech. Conf., pp. 157-158, 2002.
[25] E. A. Dengi and R. A. Rohrer, "Hierarchical 2-D field solution for capacitance extraction for VLSI interconnect modeling," in Proc. Des. Autom. Conf., pp. 127-132, 1997.
[26] Bau-Jy Liang, Don-Gey Liu, Hsiao-Chun Chen, Yu-Chen Fang, Pi-Fang Hung, "A Quick Field-Based Calculation for the Capacitances of Symmetrical Patterns in Touch Panels," J. Disp. Tech., vol. 12, no. 12, pp. 1629-1637, 2016.
[27] Wei Zhao, Xia Li, Sam Gu, Seung H. Kang, Matthew M. Nowak, and Yu Cao, "Field-Based Capacitance Modeling for Sub-65-nm On-Chip Interconnect," IEEE Trans. Electron Dev., vol. 56(9), pp.1862-1872, 2009.
[28] W. Zhao , X. Zhu , W. Deng , J. He, A. Chen and M. Chan "Field-based capacitance modeling for sub-65 nm on-chip interconnect", 2012 4th Asia Symposium Quality Electronic Design (ASQED), pp.110 -116 2012.
[29] J. Zou, Q. Xu, J. Luo, R.S. Wang, R. Huang, and Y.Y. Wang, "Predictive 3-D Modeling of Parasitic Gate Capacitance in Gate-all-Around Cylindrical Silicon Nanowire MOSFETs", IEEE Trans. Electron Device, vol. 58, no. 10, pp. 3379-3387, Oct. 2011
[30] Hsiao-Chun Chen, "Analytical solution on the pattern of projected touch panel," Master Thesis, Feng Chia University, 2013.
[31] Chia-Hung Yeh, "Analytical Solution Improvement on Capacitance Pattern for Projective Capacitance Touch Panel," Master Thesis, Feng Chia University, 2013.